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(54) Multi-address space control method and system.

(57) A multi-address space control for use in an information processing system includes accessing a plurality of address spaces (19, 22) produced by different address translation tables based on a selection command (7) for a plurality of leading address registers (5, 6), and comparing (12) a program status word (PSW) key (P_k, 1) with a main storage key (M_k, 11) in a main storage to protect the main storage. The multi-address space control between different address spaces includes a PSW key register for holding the program status work key, a work access key register (2, W_k) capable of arbitrarily designating an access key in accordance with a data transfer instruction, access means for allowing an access to the main storage irrespective of the value of a main storage key (M_k) when the valu of the key selected by a selector (3) as an access key from the work access key r gister and the PSW key register is a predetermined value (K=0), and setting means for accessing the different address spaces by changing-over the plurality of leading address registers and the work access key register and PSW register, detecting an access exception, and setting the predetermined value in the work access key register to judge the work access key as an access key if an access exception is not detected.

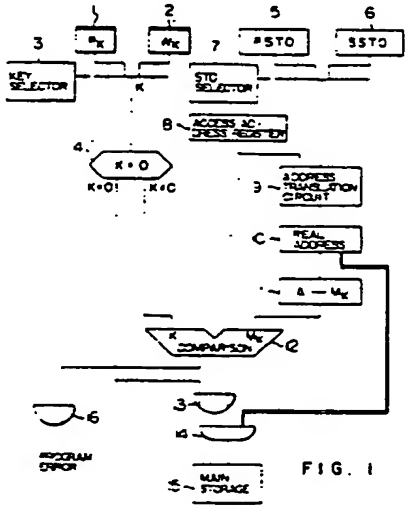

FIG. 1

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MULTI-ADDRESS SPACE CONTROL METHOD AND SYSTEM

BACKGROUND OF THE INVENTION

The present invention relates to multi-address space control and more particularly to a multi-address space control method and system suitable for the transfer of data between different address spaces.

As the instructions for the data transfer between two virtual address spaces (herein called first space and second space) produced by different address translation tables, there are known, for example, MVCP (Move to Primary) and MVCS (Move to Secondary) instructions as disclosed in IBM System/370 Principles of Operation GA22-7000-8. A MVCS instruction will be explained in the following:

With a MVCS instruction, data in the first space are transferred to the second space. For accessing the first space, a storage protect check is executed using a program status word (PSW) key. For accessing the second space, a key-controlled protection check is executed using a second space access protection key (called hereinafter a second space key) in a general register (GR) designated by an instruction operand.

A MVCS instruction in conventional systems has been processed as in the following:

According to a first scheme in conventional systems, at the step of accessing the second space, address translation is conducted by changing the contents of an address translation table leading address (hereinafter called a segment table origin (STO)) register.

After a real address for the second operand address of the first space is obtained, a real address for the first operand address of the second space is obtained using the above-described second space access step. Using the obtained real address, a data transfer from the first to the second space is performed.

However, if an operand address designates a plurality of pages, it is necessary that the operand address be translated into a real address for each page and that an access exception be checked for each page whether it is detected or not. The access exception includes a translation designation exception, segment translation exception, page translation exception, addressing exception, key control protection exception, page protection exception, lower address protection exception and no implemented memory. Further, it is necessary to store a logical address for notifying an access interruption when an access exception is detected or a program event is to be interrupted, thus resulting in complicated processing.

According to a second scheme in conventional systems, second operand data in the first space are sequentially read and temporarily stored in a hardware work area. The second space access step described in the above first scheme is executed and thereafter, the data in the work area are sequentially written in the second space. However, a work area having a space as large as the data length to be transferred is required. Further, the transfer operation of operand data is not executed through repetition of second-operand read operation and first-operand write operation so that the processing speed is lowered in some cases.

In both first and second schemes, a PSW key is changed to a second space key to access the second space for storage protection check. Further, if an interruption occurs during data transfer, it is necessary to immediately set the contents of the address translation table top address at an initial value. Particularly for processing a MVCP or MVCK instruction, when an interruption occurs in both schemes while a PSW key is changed to a second space key, it is necessary to immediately set the program status word at an initial value. Furthermore, it is necessary to change a program status word every time a different address space is accessed, thereby resulting in complicated processing and low processing speed.

Schemes of this type are disclosed, for xample, in JP-A-57-8860, and US-A-4,521 846 (JP-B-60-41379).

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a multi-address space control method and system, for use in processing data transfer between different address spaces, capable of reducing the number of steps of protection key processing to enable a high speed data transfer.

It is another object of the present invention to provide multi-address space control obviating the necessity of changing a program status word key while accessing a different address space.

According to one aspect of the present invention, there is provided a multi-address space control system for use in an information processing system for accessing a plurality of address spaces generated by different address translation tables based on a selection command for a plurality of

leading address registers, and comparing a program status word key with a storage key in the main storage to protect the main storage, the multi-address space control system including: a PWS key register for the program status word (PSW), a work access key register capable of arbitrarily designating an access key, means for allowing an access to the main storage irrespective of the storage key value when the access key selected from the two keys of the access key registers has a predetermined value (K=0), rehearsal enabling means for accessing the different address spaces by changing the plurality of leading address registers and the two access key registers, detecting an access exception, and if no access exception is detected, setting the predetermined value in the work access key register, and selector means for selecting the work access key register value as an access key and allowing data transfer between different address spaces.

According to an operational aspect of this invention, STOs for the first and second spaces are set in the PWS key register and the work access key register, respectively. Microprograms or suitable hardware is constructed such that the PWS key register and the work access key register are selected as STOs for the cases of accessing the first and second spaces, respectively, to change a space.

An arbitrary access key value can be set as desired in a work access key register provided independently from a PSW key register. The selection of one of the PSW key and the work access key can be instructed by a selector to check storage protection.

As a result, it is not necessary to change the STO register and the PSW key independently of whether an access to the first or to the second space is intended.

The following advantages are achieved with the embodiments of this invention:

A main storage can be accessed while satisfying main storage protection and not changing a PSW key of the CPU. Thus, complicated processing of changing a PSW can be omitted.

In transferring data between main storages having different main storage keys, a key protection exception can be suppressed by selecting a work access key selection mode and setting the work access key "0", to thereby allow accessing by the same access key and thus enable a high speed data transfer.

Since an address space can be changed easily, there is no need of changing a STO, thus enabling a high speed data transfer between address spaces.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an embodiment of a data processing system according to the present invention;

Fig. 2 shows where keys for managing main storage protection are located;

Fig. 3 is a flow chart showing the processing for a data transfer instruction between different address spaces;

Fig. 4 is a flow chart showing another embodiment of the processing for a MVCP instruction according to the present invention;

Fig. 5 is a flow chart showing another embodiment of the processing for a MVCK instruction; and

Figs. 6A and 6B are diagrams for explaining the difference between the present invention and a conventional system.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail with reference to the accompanying drawings.

Fig. 1 is a block diagram showing an embodiment of a data processing system according to th present invention.

In the Figure, a single program status word (PSW) present in a central processing unit includes a PSW key which is registered in a PSW key register 1 (PSW key is called "P_k"). A work access key register (work access key is called "W_k") is provided independently from the PSW key register 1. A key selector 3 selects, under microprogram control, one of the PSW key register 1 and the work access key register 2. A judgement circuit 4 judges if a key from the key registers selected by the key selector 3 is "0" or not. There are also provided a first address translation table l ading address register 5 (called a "PSTO") and a second address translation table leading address register 6 (called an "SSTO"). A STO selector 7 selects one of PSTO 5 and SSTO 6. A logical address register 8 loads a logical address of a main storage 15 to be accessed. An address translation circuit 9 translates a logical address in the logical address register 8 into a real address. A real address output circuit 10 controls the output of the address translation circuit 9 to provide a real address. A read circuit 11 reads a storage key $M_k$corresponding to an address outputted from the real address output circuit 10. A comparator circuit 12 compares a main storage key M_k read by the read circuit 11 with a selected key K (not zero). An access enable signal generator 13 generates an access enable

signal. Upon reception of an access enable signal from the access enable signal generator 13, a main storage access circuit 14 accesses a main storage 15 storing various data, based on address data from the real address output circuit 10. An error notification circuit 16 sends to a hierarchical unit (not shown) a program error signal when the comparator circuit 12 outputs a non-coincidence result.

Fig. 2 is a schematic diagram showing where keys for managing main storage protection are located, wherein identical numbers to those in Fig. 1 represent similar elements and parts.

Referring to Fig. 2, there are shown a program status word 17, a first address space 19 (PS) produced by PSTO 5, a main storage key 20 (PS_k) corresponding to a first address space 19, a second address space 22 (SS) produced by SSTO 6, a main storage key 23 (SS_k) corresponding to SSTO 6, and an instruction format 24 (hereinafter called "instruction"). Each data is stored in a register or a memory.

In the embodiment shown in Fig. 2, the specification of a data transfer instruction 24 is as follows:

"A second operand on the first address space 19 is read or fetched using a PSW key P_k, to thereafter write i.e., store a key value X_k given by the instruction as an access key K in the second address space 22 different from the first address space. The lengths of first and second operands are both L bytes. When the access key K and a storage key M_k do not coincide with each other and the access key K is not "0", a program error is detected and a data transfer instruction is suppressed."

In this embodiment, it is assumed that an address translation table leading address for use in producing a first address space 19 (PS) and that for a second address space 22 (SS) are stored beforehand in PSTO 5 and SSTO 6, respectively.

Fig. 3 is a flow chart showing processings executed by microprograms or the like, of a data transfer instruction between different address spaces. The data transfer operation between different address spaces will be described using the instruction 24 shown in Fig. 2 as an example, with reference to Fig. 1 and the procedure shown in Fig. 3.

(i) A store rehearsal is first prepared to judge if a program error will be detected while a first operand is stored. A key value X_k supplied from the instruction 24 on the CPU side is set in the work access key register 2, and an output selection command for the work access key register 2 is given to the key selector 3. In the following, a key selected by the key selector 3 using a key value X_k is referred to as "K". A first operand address generated from the instruction 24 is set in the logical address register 8 as an address to be accessed. The first operand is located in the second address space 22 (SS) generated through address translation using SSTO 6 as an address translation table leading address (hereinafter called "STO"), and accordingly, the STO selector 7 is caused to select SSTO 6 as a STO (step 25).

(ii) A store rehearsal for the first operand is executed. The first operand address (the logical address) set at the access logical address register 8 is translated into a real address 10 by the address translation circuit 9. The corresponding storage key or space 23 (SS_k) added to the second address space 22 is read by the read circuit 11. In the meantime, the judgement circuit 4 judges if a key K ($=X_k$) selected by the key selector 3 is "0" or not. If the judgement results in K=0, the main storage key M_k, i.e., SS_k is not compared with the access key K, to allow an access to the main storage 15. K=0, accordingly, represents a so-called "almighty key" which allows an access to the main storage 15 arbitrarily without any requirements. If the access key K selected by the selection circuit 3 is not "0", the comparator circuit 12 compares the access key K with the storage key M_k read by the read circuit 11. If a comparison result by the comparator circuit 12 shows $K=M_k$, i.e., $X_k=SS_k$, then an access enable signal is generated which is applied via the access enable signal gate 13 and the main storage access circuit 14 to the main storage 15 for the access ther of. Since the store rehearsal is executed at this time, the access circuit 14 is controlled by microprograms to prevent writing into the main storag 15. If K does not match M_k, i.e., X_k is not equal to SS_k, the comparator circuit 12 generates and sends a program error signal to the error notification circuit 16 (steps 26 and 26A). In this case, the processing terminates as an abnormal state.

(iii) For the preparation of a fetch rehearsal, the access key value X_k supplied from the instruction 24 is set in the W_k register 2. The key sel ctor 3 is given a selection command for selecting an output from the PSW key (P_k) register 1. Since a second operand is located in the first address space 19 (PS) generated by address translation using PSTO 5 as the address translation table leading address, the STO selector 7 is controll d, for example, by execution of microprograms to select PSTO 5 (step 27).

(iv) Similarly to the above step (ii), a fetch rehearsal for the second operand is executed. If a access key $K=P_k$ (PSW key) selected by the key selector 3 is "0", a success of a fetch rehearsal is assumed. If K is not "0" and coincides with the storage key or space 20 (PS_k) added to the first address space 19 (PS), i.e., $K=PS_k$, an access to the main storage 15 is possible so that a success

of a fetch rehearsal is assumed.

If K is not "0" and does not coincide with M_k, i.e., P_k is not PS_k, a program error is assumed to suppress the instruction (steps 28 and 28A). In case of instruction suppression, the processing is terminated as an abnormal state.

(v) After a success of a fetch rehearsal, $W_k = 0$ is set in the W_k register 2, and a selection command for the work access key is given to the key selector 3 (step 29).

(vi) A process for reading a operand data from the first address space 19 and writing them to the second address space 22 is performed. A selection command for an STO issues simultaneously with a main storage access request. Microprograms give an access instruction to PSTO 5 to be selected as a STO when the data is fetched from the first address space 19, and give an access instruction to SSTO 6 to be selected as a STO when the data are stored in the second address space 22. Although the storage key is read, comparison of the storage key with the access key is not effected because the access key is "0". Thus, irrespective of the value of the storage key, an access to the storage is allowed (steps 30, 31).

(vii) It is judged if the data transfer between the first and second address spaces has been completed up to L bytes. The above step (vi) is repeated until the transfer up to L bytes is completed (step 32).

(viii) After the end of data transfer processing, a selection command for the PSW key P_k is given to the key selector 3 to resume a status before execution of an instruction (step 33).

(ix) If a program error is detected, the operation is set at an output selection mode for the PSW key register to initiate an interruption process.

In the similar manner as above, the present invention is applicable to a MVCP or a MVCK instruction.

According to the specification of an MVCP instruction, a second operand in the second address space is read using the key value X_k supplied from the instruction, and is written into a first-operand address in the first address space using the PSW key P_k as the access key. The lengths of the first and second operands are both L bytes. When the access key K is not "0" and does not coincide with the main storage key M_k, a program error is detected and the instruction is suppressed.

Fig. 4 is a flow chart showing an example of data transfer by a MVCP instruction. In a store operation for a first operand in the second address space 22 (SS), PSTO register 5 is set at a selection mode (step 35) to effect a store rehearsal for the first operand (step 36). Next, the key selector 3 is set at a selection mode for the W_k register 2 in which a key value X_k given by the MVCP instruction has been set. The STO selector 7 is set so as to select the SSTO register 6 (step 37). Thereafter, a fetch rehearsal for a second operand is conducted (step 38). Upon success of a fetch rehearsal, the W_k register 2 is set "0" (step 39). A processing of fetching data from the second address space 22 in the SSTO selection mode and storing it in the first address space 19 in the PSTO selection mode is performed (steps 40, 41). The following operation is identical to steps 32 and 33 of the embodiment described before.

Fig. 5 is a flow chart showing an embodiment of the present invention to which an MVCK instruction is applied. Steps similar to those of the preceding embodiment are designated by same reference numbers.

The specification of an MVCK instruction can be decided as in the following example: A second operand is read using the key value X_k suppli d from a MVCK instruction. The PSW key P_k is written in as an access key K at the first operand address. The lengths of the first and s cond operands are both L bytes. If K is not "0" and does not coincide with M_k, a program error is detect d and the MVCK instruction is suppressed to be executed.

Particularly, with a MVCK instruction, a STO is selected in accordance with an address space control bit in the PSW. W_k is used as an access k y for fetching a second operand, while the PSW key P_k is used as an access key for storing a first operand. Consequently, selection modes for PSTO and SSTO as in the embodiments described before are not needed as illustrated in steps 47, 50 and 51.

Data transfer according to the present invention and a prior art will be compared with reference to the timing charts shown in Figs. 6A and 6B.

In the case where a request address is given by a logical address, the following operations are generally performed for each fetch (or store)-operation:

(1) recognizing a request address,

(2) judging if the request address is pr sent in a translation lookaside buffer (TLB),

(3) deriving a real address from the TLB if the request address is present in it,

(4) deriving a real address through address translation if the request address is not present in the TLB, and

(5) fetching (or storing) data from (or into) a storage or a cash memory at the real address using an access key.

If the same acc ss key K is used to repeat a request, the above operations can be generally executed in an overlap manner.

Fig. 6A shows a timing chart of a read/write operation using the same access key. In the Figure, fetch and store operations are executed in an overlap manner, which are realized through a pipeline processing of the above operations (1) to (5).

However, in transferring data between address spaces by different access keys, an access key value X_k different for each request must be used. In such a case, the access key value K must be maintained unchanged until the above operation (5) is completed. Therefore, a request has been processed heretofore serially as shown in Fig. 6B by way of the operations ⓐ and ⓑ by which a PSW key is changed to a corresponding address space key.

In contrast with the above, in the embodiments according to the present invention, K=0, i.e., almighty access is used in data transfer between address spaces even if they have different keys. Therefore, the data transfer between address spaces is performed using an apparently same access key, thus enabling an overlap among the accesses as shown in Fig. 6A and a high speed data transfer.

Claims

1. An information processing method including accessing a plurality of address spaces (19, 22) produced by different address translation tables (9) based on a selection command (7) for a plurality of leading address registers (5, 6), and comparing (12) a program status word (PSW) key (P_k, 1) with a main storage key (M_k, 11) to thereby protect a main memory, comprising, in a data transfer between different access spaces, the stpes of:

(a) setting a work access key (W_k) capable of being designated in accordance with an instruction to be executed, independently from said program status word key;

(b) selecting as an access key (K) on the side of a central processing unit one of said program status word (PSW) key (P_k) and said work access key (W_k);

(c) if the selected access key is at a predetermined value (K=0), allowing an access to said main storage irrespective of said main storage key value; and

(d) accessing different address spaces by changing said plurality of leading address registers, PSW key (P_k) and word access key (W_k), detecting an access exception, and if an access exception is not detected, setting said predetermined value (K=0) as an access key in said work access key.

2. A method according to claim 1, wherein each of said steps is executed under control of microprograms, said steps constituting a pre-testing (rehearsal) for setting an access key to be prepared on the central processing unit side.

3. A method according to claim 1, wherein said access exception includes translation specification exception, segment translation exception, page translation exception, addressing exception, and protection exception.

4. A method according to claim 1, wherein said step (c) includes a step of inhibiting actual accessing to said main storage.

5. A method according to claim 2, wherein said step (d) includes a store rehearsal for an address space to which a data is transferred and a fetch rehearsal for an address space from which a data is transferred.

6. An information processing system wherein a plurality of address spaces (19, 22) produced by different address translation tables based on a selection command for a plurality of leading address registers (5, 6) are accessed, and a program status word key (P_k) and a storage key (M_k) are compared to protect a main storage, having

a multi-address space control system comprising:

a first key register (1) for holding said program status word key;

a second key register (2) for holding a work access key variably designated in accordance with an instruction to be executed;

a key selector (3) for selecting said first and second key registers;

judging means (4) coupled to the output of said key selector (3) for judging whether the value of key selected from said first and second key registers is a predetermined value (K=0), and enabling an access to said main storage irrespective of the value of said storage key if said selected key value is equal to said predetermined value; an

means (12, 16, 4, 3, 2) for accessing different address spaces by changing said plurality of leading address registers, and said first and second key registers, detecting an access exception, and setting, if an access exception is not detected, said predetermined value in said second key register as an access key for use in transferring data between different address spaces.

7. An information processing system for a multi-address space control wherein when a main storage is to be accessed from a central processing unit, a main storage protection is conducted by comparing an access key prepared in said central proc ssing unit with a main storage key provided in the main storage, comprising:

a first key register (1) for storing a program status word key prepared in said central process-

ing unit;

a second key register (2) for storing an access key designated in accordance with a data transfer instruction;

a selector (3) for selecting one of the outputs from said first and second key registers;

judging means (4) coupled to said selector for comparing a key value from a selected key register with a predetermined value, allowing an access to said main storage irrespective of said main storage key when the key value of said selected key register matches said predetermined value, and making the key value of said selected key register to be compared with said main storage key; and

means including a microprogram for executing a predetermined procedure, for setting said predetermined value in said second key register as an access key for data transfer between a plurality of address spaces when a key included in a transfer instruction coincides with said main storage key.

8. A system according to Claim 6, wherein said instruction is a data transfer instruction, one of first and second operands is fetched and stored into the other operand address, the access key (P_k) for said one of first and second operands is designated by said program status instruction and the access key (W_k) for the other of the first and second operands is designated by said data transfer instruction.

9. A system according to Claim 8, wherein said key selector (3) selects one of the outputs of said first and second key registers (1, 2) by a microprogram associated with said data transfer instruction.

10. A system according to Claim 6, wherein said first key register (1) holds an access key to detect an access exception for one of first and second operands and said second key register (2) holds a key given by a data transfer instruction as an access key to detect an access exception for the other of said first and second operands.

11. A system according to Claim 6, wherein said second key register (2) is set at a key value always available to access for transfer of first and second operands of a predetermined unit length through repetitive fetch and store operations.

FIG. 1

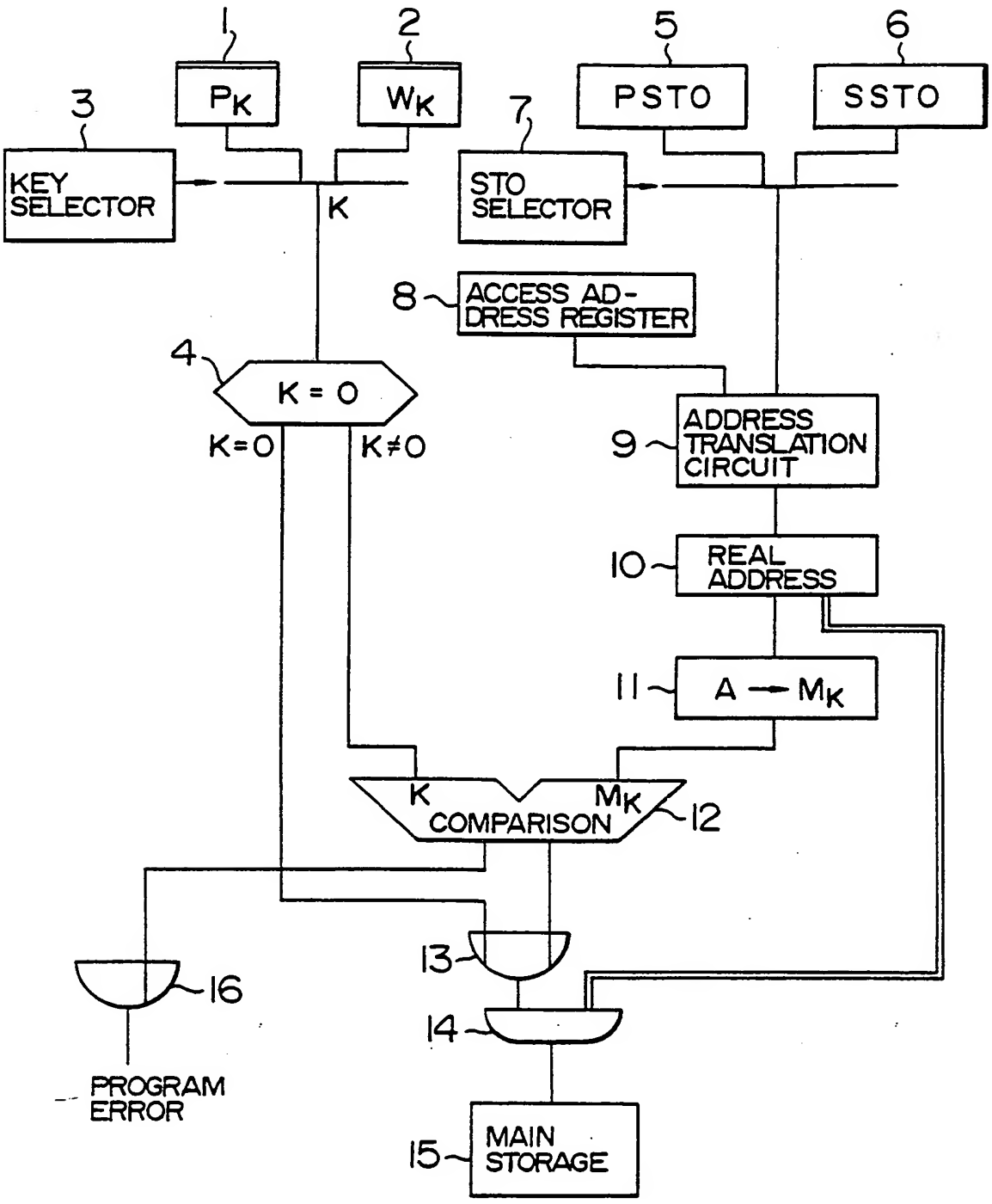
1
2
5
6
3
PK
WK
PSTO
SSTO
KEY SELECTOR
K
7
STO SELECTOR
8
ACCESS ADDRESS REGISTER
4
K = 0
K=0
K≠0
9
ADDRESS TRANSLATION CIRCUIT
10
REAL ADDRESS
11
A → MK
K
MK
COMPARISON
12
13
16
14
PROGRAM ERROR
15
MAIN STORAGE

FIG. 2

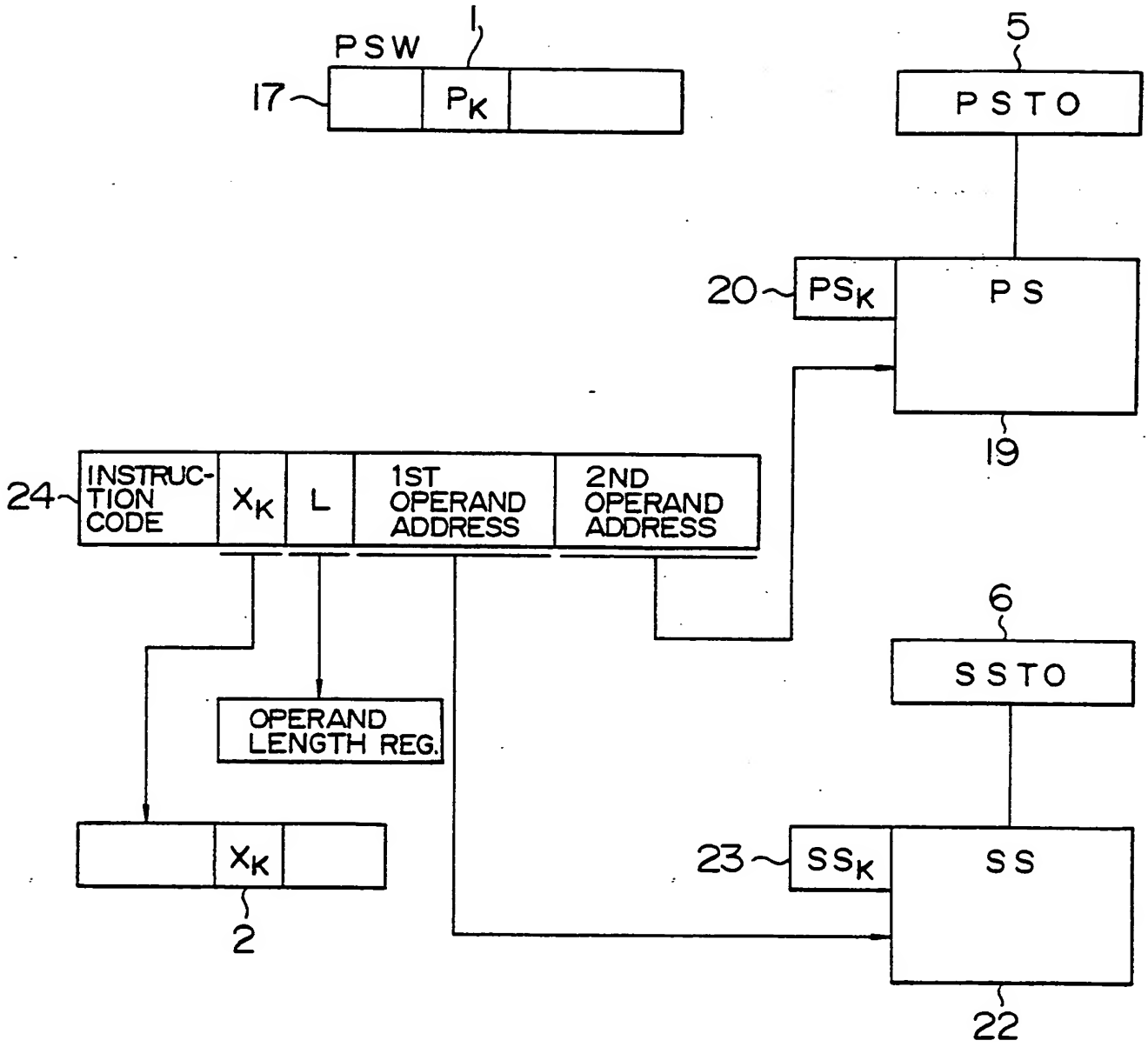
PSW
1
17
PK
5
PSTO
20
PSK
PS
19
24
INSTRUC-TION CODE
XK
L
1ST OPERAND ADDRESS
2ND OPERAND ADDRESS
6
SSTO
OPERAND LENGTH REG.
XK
2
23
SSK
SS
22

FIG. 3

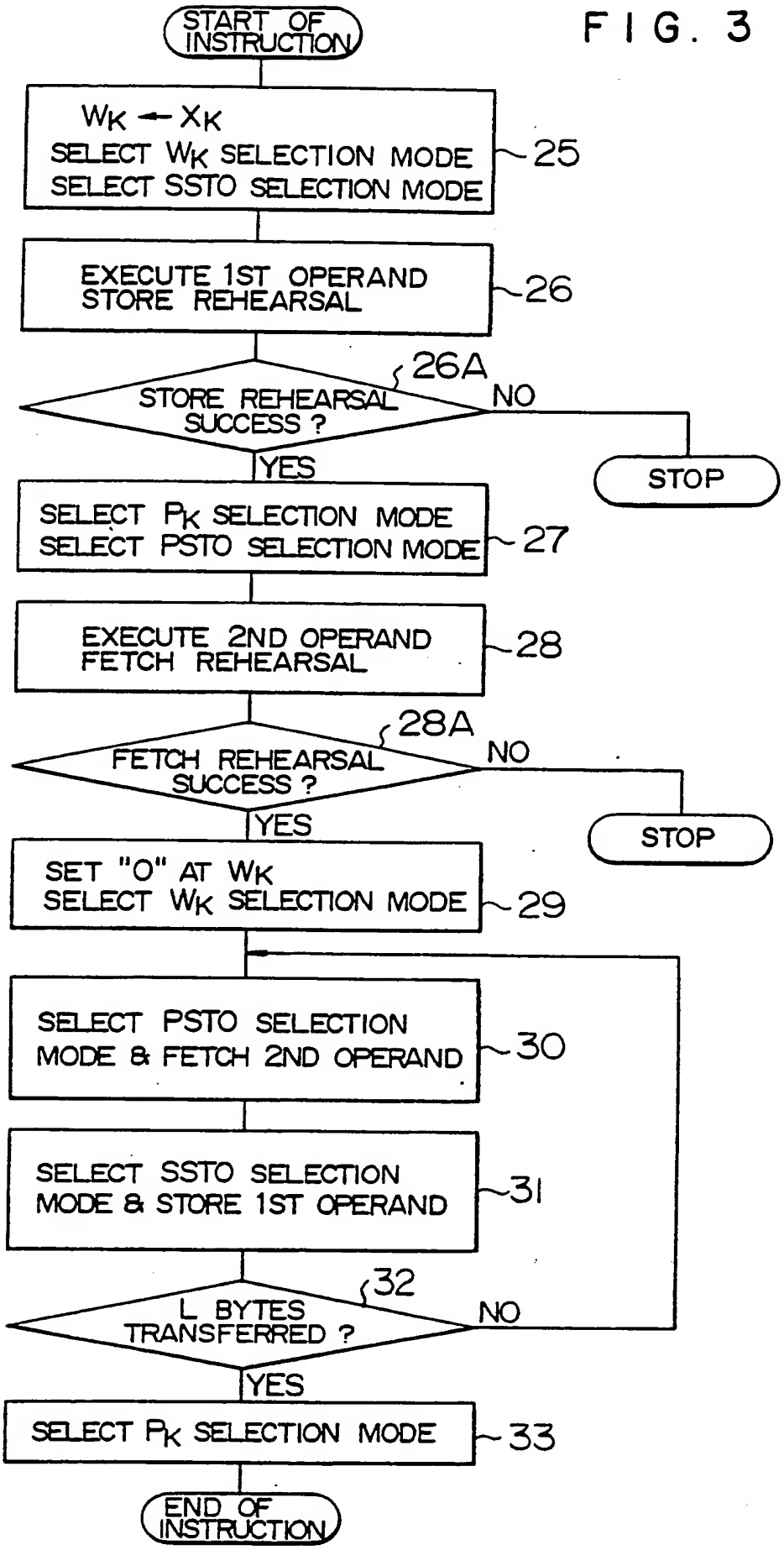
START OF INSTRUCTION
$W_K \leftarrow X_K$
SELECT W_K SELECTION MODE
SELECT SSTO SELECTION MODE
25
EXECUTE 1ST OPERAND STORE REHEARSAL
26
STORE REHEARSAL SUCCESS ?
26A
NO
STOP
YES
SELECT P_K SELECTION MODE
SELECT PSTO SELECTION MODE
27
EXECUTE 2ND OPERAND FETCH REHEARSAL
28
FETCH REHEARSAL SUCCESS ?
28A
NO
STOP
YES
SET "0" AT W_K
SELECT W_K SELECTION MODE
29
SELECT PSTO SELECTION MODE & FETCH 2ND OPERAND
30
SELECT SSTO SELECTION MODE & STORE 1ST OPERAND
31
L BYTES TRANSFERRED ?
32
NO
YES
SELECT P_K SELECTION MODE
33
END OF INSTRUCTION

FIG. 4

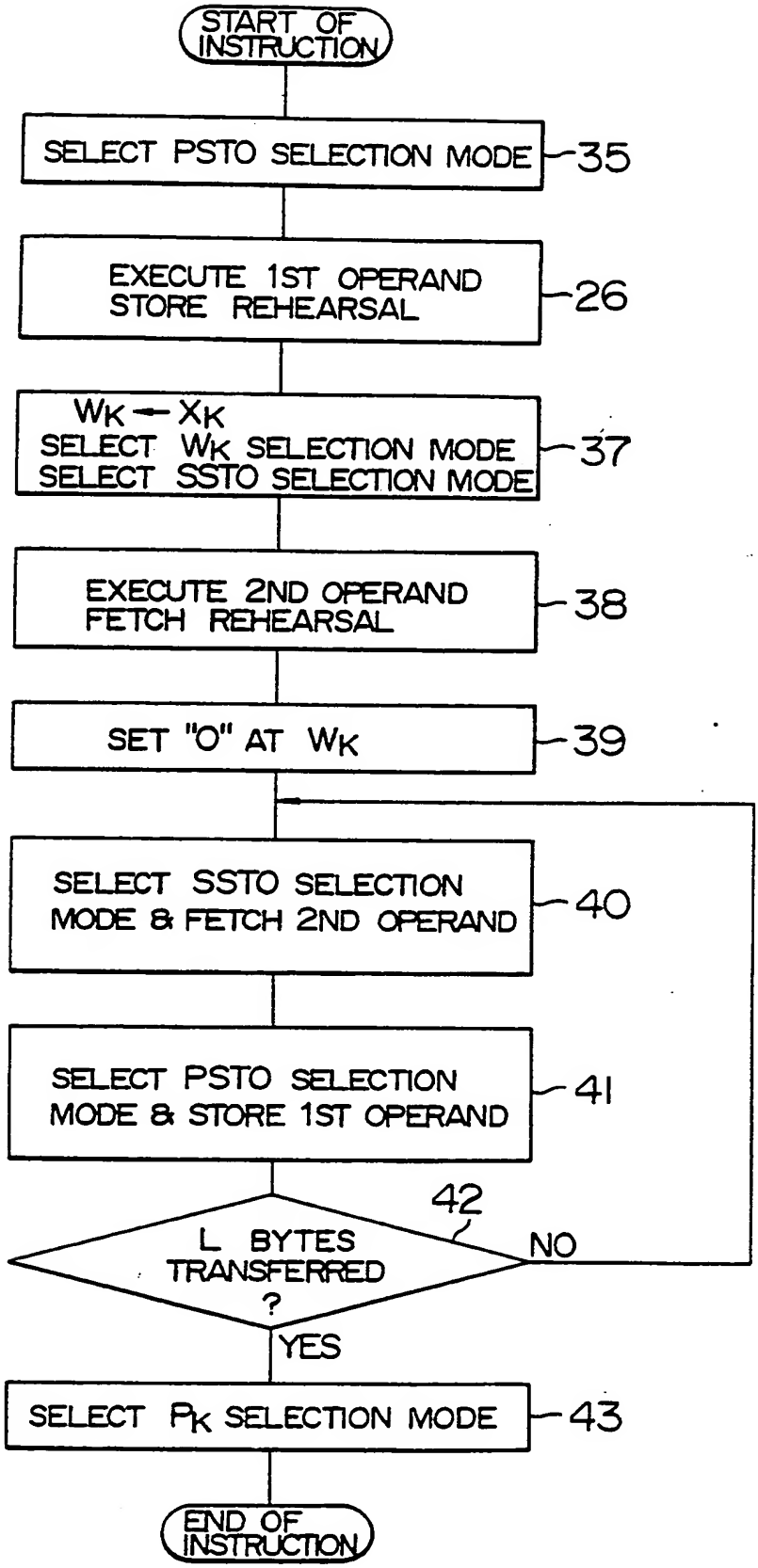
START OF INSTRUCTION
SELECT PSTO SELECTION MODE
35
EXECUTE 1ST OPERAND STORE REHEARSAL
26
$W_K \leftarrow X_K$
SELECT W_K SELECTION MODE
SELECT SSTO SELECTION MODE
37
EXECUTE 2ND OPERAND FETCH REHEARSAL
38
SET "0" AT W_K
39
SELECT SSTO SELECTION MODE & FETCH 2ND OPERAND
40
SELECT PSTO SELECTION MODE & STORE 1ST OPERAND
41
42
L BYTES TRANSFERRED ?
NO
YES
SELECT P_K SELECTION MODE
43
END OF INSTRUCTION

FIG. 5

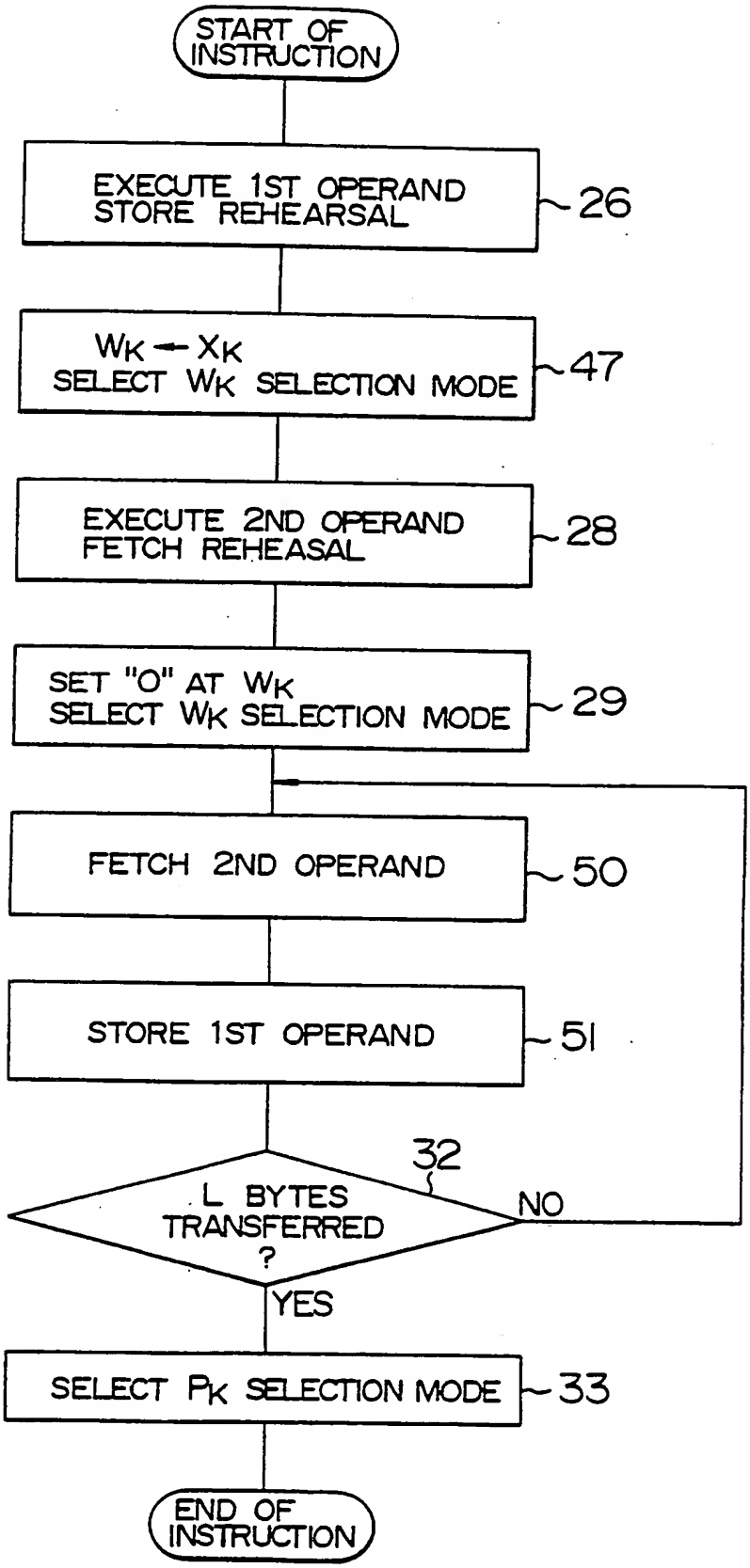
START OF INSTRUCTION
EXECUTE 1ST OPERAND STORE REHEARSAL
26
$W_K \leftarrow X_K$ SELECT W_K SELECTION MODE
47
EXECUTE 2ND OPERAND FETCH REHEASAL
28
SET "O" AT W_K SELECT W_K SELECTION MODE
29
FETCH 2ND OPERAND
50
STORE 1ST OPERAND
51
32
L BYTES TRANSFERRED ?
NO
YES
SELECT P_K SELECTION MODE
33
END OF INSTRUCTION

FIG. 6A

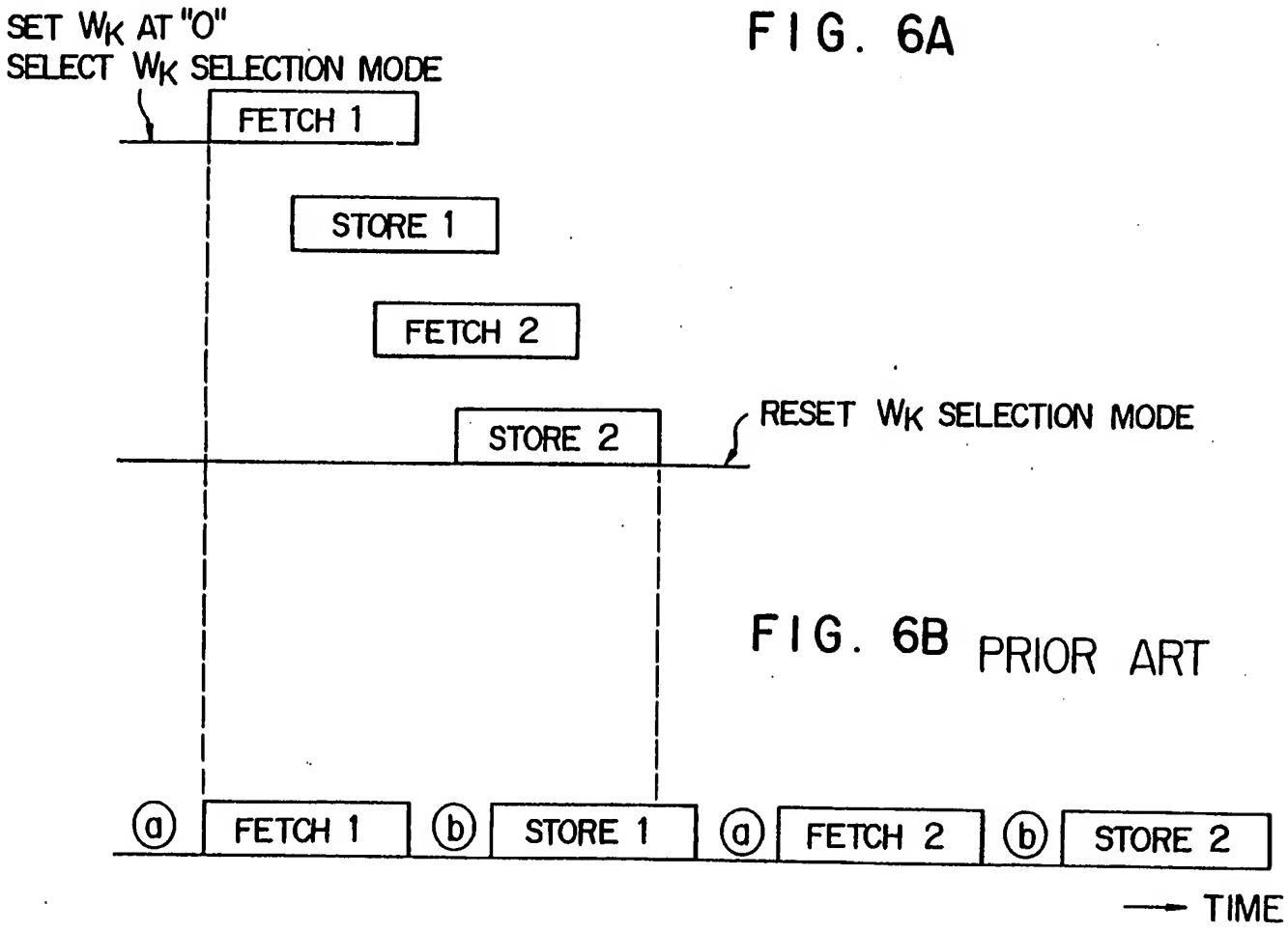

FIG. 6B PRIOR ART

ⓐ , ⓑ : OPERATION OF CHANGING PSW KEY TO EACH ACCESS KEY

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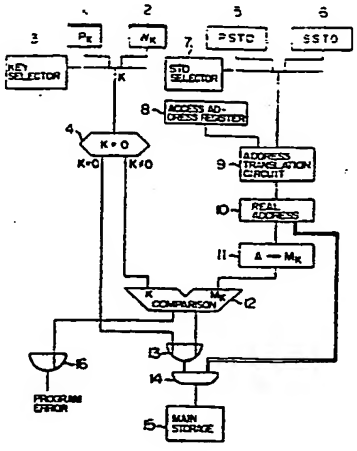
(54) Multi-address space control method and system.

(57) A multi-address space control for use in an information processing system includes accessing a plurality of address spaces (19, 22) produced by different address translation tables based on a selection command (7) for a plurality of leading address registers (5, 6), and comparing (12) a program status word (PSW) key (P_k, 1) with a main storage key (M_k, 11) in a main storage to protect the main storage. The multi-address space control between different address spaces includes a PSW key register for holding the program status work key, a work access key register (2, W_k) capable of arbitrarily designating an access key in accordance with a data transfer instruction, access means for allowing an access to the main storage irrespective of the value of a main storage key (M_k) when the value of the key selected by a selector (3) as an access key from the work access key register and the PSW key register is a predetermined value (K=0), and setting means for accessing the different address spaces by changing-over the plurality of leading address registers and the work access key register and PSW register, detecting an access exception, and setting the predetermined value in the work access key register to judge the work access key as an access key if an access exception is not detected.

FIG 1



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Application Number

EP 87 11 1608

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	EP-A-0 040 703 (IBM) * Page 1, lines 17-21; page 2, lines 12-15; page 4, line 19 - page 5, line 8; page 6, line 11 - page 7, line 3; page 8, lines 1-15; page 14, lines 8-10; page 15, lines 1-6; page 17, lines 8-22; page 24, lines 6-14; page 34, line 3 - page 35, line 12; figures 1-3,14 *	1,4,6-10	G 06 F 12/14
A		2,3,5, 11	

Y	EP-A-0 079 133 (CDC) * Figure 1; page 3, line 26 - page 6, line 15; page 7, lines 8-14; page 10, lines 7-19; page 11, lines 10-28; page 19, lines 1-15 *	1,4,6-10	
A		2,3,5, 11	

A	PATENT ABSTRACTS OF JAPAN, vol. 6, no. 70 (P-113)[948], 6th May 1982; & JP-A-57 8860 (FUJITSU K.K.) 18-01-1982	1,6,7	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
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A	EP-A-0 115 877 (IBM) * Figure 3; page 13, line 30 - page 14, line 32 *	1,6,7	

A	PROCEEDINGS OF 24th NATIONAL CONFERENCE, August 1969, pages 419-429, New York, US; S. MOTOBAYASHI et al.: "The HITAC5020 time sharing system" * Page 420, right-hand column, line 32 - page 421, left-hand column, line 3; figure 4 *	1,6,7	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07-12-1989	MASCHE C.M.

CATEGORY OF CITED DOCUMENTS

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